Application No. 10/602436
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CLMPTO
CLAIMS 1-11 (CANCELLED)

Claim 12 (previously presented). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate having a silicon surface having a silicon-containing multilayer on an insulator layer;

a1) depositing a layer of SiGe onto the silicon on insulator substrate, the deposited SiGe having a parallel lattice constant in the directions parallel to the silicon surface and a perpendicular lattice constant in the direction perpendicular to the silicon surface,

wherein the parallel lattice constant being similar to the lattice constant of silicon and the perpendicular lattice constant being greater than the parallel lattice constant;

b) patterning the silicon and the SiGe multilayer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure having a parallel lattice constant and a greater perpendicular lattice constant;

c) depositing an epitaxial channel layer onto the seed fin structure, the channel layer material having a lattice constant smaller than that of the perpendicular lattice constant seed fin material, wherein the epitaxial channel layer becomes a tensile strained channel layer in the direction perpendicular to the silicon surface due to the lattice mismatch between the channel layer and the seed fin structure;

d) forming a gate dielectric layer on the epitaxial strained channel; and

e) forming a gate over the epitaxial strained channel.

Claim 13-14.(canceled)

Claim 15 (currently amended). [[A]] <u>The</u> method as in claim 12 wherein the germanium content of the silicon germanium layer seed fin is between 10% to 100%.

Claim 16 (currently amended). [[A]] <u>The</u> method as in claim 12 wherein the epitaxial channel layer is a silicon layer, a silicon germanium layer, a carbon doped silicon layer, or a carbon doped silicon germanium layer.

Claim 17 (currently amended). [[A]] The method as in claim 12 wherein the patterning of the source, drain and channel regions from the multilayer comprises the steps of:

b1) providing a patterned mask on the multilayer;

b2) patterning the multilayer according to the patterned mask to define source, drain and channel regions; and

b3) removing the patterned mask.

Claim 18 (currently amended). [[A]] The method as in claim 12 further comprising a step c1 after step c:

c1) doping the channel region.

Claim 19 (currently amended). [[A]] The method as in claim 12 wherein the formation of the gate comprises the steps of:

e1) depositing a gate material layer;

e2) doping the gate material layer;

e3) providing a patterned mask on the gate material layer;

e4) patterning the gate material layer according to the patterned mask to define the gate; and

e5) removing the patterned mask.

Claim 20 (currently amended). [[A]] The method as in claim 12 further comprising a step f after step e:

f) forming lightly doped region (LDD) and halo regions between the channel region and the source and drain regions.

Claim 21 (currently amended). [[A]] The method as in claim 12 further comprising the following steps after step e:

g) forming dielectric spacers between the gate and the source and drain regions.

h) doping the source and drain regions.

i) forming salicide of the gate, source and drain regions.

Claim 22-23 (canceled)

Claim 24 (currently amended). [[A]] The method as in claim 12 wherein the thickness of the first silicon-containing layer of the silicon on insulator substrate is between 5 nm to 20 nm.

Claim 25 (canceled).

Claim 26 (currently amended). [[A]] The method as in claim [[25]] 12 wherein the germanium content of the silicon germanium layer is between 10% to 50%.

Claim 27 (currently amended). [[A]] The method as in claim 12 further comprising the following step after step a1)

a2) depositing wherein the top most layer of the multilayer comprises a hard mask layer onto the SiGe layer.

Claim 28 (currently amended). [[A]] The method as in claim 12 wherein the height of the seed fin structure is between 10 nm to 200 nm.

Claim 29 (currently amended). [[A]] The method as in claim 12 wherein the width of the seed fin structure is between 5 nm to 100 nm.

Claim 30 (currently amended). [[A]] The method as in claim 12 wherein the thickness of the strained channel layer is between 5 nm to 15 nm.

Claim 31-41. (canceled)

Claim 42 (previously presented): A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate having a silicon surface;

a1) depositing a layer of SiGe onto the silicon on insulator substrate, the deposited SiGe having a parallel lattice constant in the directions parallel to the silicon surface and a perpendicular lattice constant in the direction perpendicular to the silicon surface,

wherein the parallel lattice constant being similar to the lattice constant of silicon and the perpendicular lattice constant being greater than the parallel lattice constant;

b) patterning the silicon and the SiGe multilayer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure having a parallel lattice constant and a greater perpendicular lattice constant;

c) depositing an epitaxial silicon channel layer onto the seed fin structure, wherein the epitaxial silicon channel layer becomes a tensile strained silicon channel layer in the direction perpendicular to the silicon surface due to the lattice mismatch between the silicon channel layer and the seed fin structure;

d) forming a gate dielectric layer on the epitaxial strained channel; and

e) forming a gate over the epitaxial strained channel.